WHAT IS CLAIMED IS:

1. A solid-state imaging device comprising:

an imaging area having unit cells arranged in a two-dimensional fashion on a semiconductor substrate, each of the unit cells including first and second photoelectric conversion/storage sections for photoelectrically converting incident light and storing charges thus generated, first and second charge readout circuits for transferring charges stored in the first and second photoelectric conversion/storage sections to a common charge detecting section, a potential detecting circuit for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines, a reset circuit for discharging the charges transferred to the charge detecting section, and an address circuit for selectively activating the potential detecting circuit;

a vertical driving circuit provided in correspondence to each pixel row of said imaging area, for driving the first and second charge readout circuits, reset circuit and address circuit of each of the unit cells at preset timings;

signal processing circuits respectively attached to the vertical signal lines which are provided for respective columns of the unit cells, for performing

required signal processes;

a horizontal driving circuit for scanning outputs of said signal processing circuits in a horizontal direction at preset timings to detect the same; and

an output circuit for outputting output signals of said signal processing circuits detected by the scanning operation by said horizontal driving circuit;

wherein the solid-state imaging device has a first operation mode in which the first and second charge readout circuits are driven at substantially the same timing by said vertical driving circuit, the charges stored in the first and second photoelectric conversion/storage sections are transferred to and added together in the charge detecting section, and the potential detecting circuit detects the added charges, generates and transmits a potential corresponding to an amount of detected charges to the vertical signal line, and outputs the potential from said output circuit via said signal processing circuits.

2. The solid-state imaging device according to claim 1, which further comprises a pixel row selection switching section for controlling said vertical driving circuit based on a signal for specifying the first operation mode and a signal for specifying a second operation mode and in which the first and second charge readout circuits are driven by said vertical driving circuit at substantially the same timing in the first

operation mode and the first and second charge readout circuits are driven by said vertical driving circuit at different timings in the second operation mode.

3. The solid-state imaging device according to claim 1, wherein said vertical driving circuit includes a pulse generating section for outputting an address pulse, first and second readout pulses and reset pulse.

4. The solid-state imaging device according to claim 1, wherein each of said signal processing circuits includes a noise canceller circuit.

5. A solid-state imaging device comprising:

an imaging area having unit cells arranged in a two-dimensional fashion on a semiconductor substrate, each of the unit cells including a photoelectric conversion/storage section for photoelectrically converting incident light and storing charges thus generated, a charge readout circuit for transferring charges stored in the photoelectric conversion/storage section to a charge detecting section, a potential detecting circuit for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines, a reset circuit for discharging the charges transferred to the charge detecting section, and an address circuit for selectively activating the potential detecting circuit;

a vertical driving circuit provided in correspondence to each pixel row of said imaging area, for driving the charge readout circuit, reset circuit and address circuit of each of the unit cells at preset timings;

signal processing circuits respectively attached to the vertical signal lines which are provided for respective columns of the unit cells, for performing required signal processes;

horizontal readout switching circuits for controlling transfer of outputs of said signal processing circuits corresponding to the respective vertical signal lines to a horizontal signal line;

a horizontal driving circuit for controlling said horizontal readout switching circuits at preset timings; and

an output circuit for outputting output signals of said signal processing circuits which are read out to the horizontal signal line by controlling said horizontal readout switching circuits by use of said horizontal driving circuit;

wherein the solid-state imaging device has a first operation mode in which said horizontal driving circuit sequentially turns ON said horizontal readout switching circuits in correspondence to the vertical signal lines to sequentially output the output signals of said signal processing circuits corresponding to the

vertical signal lines from said output circuit via the horizontal signal line and a second operation mode in which said horizontal driving circuit turns ON said horizontal readout switching circuits corresponding to a plurality of vertical signal lines at substantially the same time to read out the output signals of said signal processing circuits corresponding to the plurality of vertical signal lines to the horizontal signal line, average the output signals, and output the averaged output signal from said output circuit.

6. The solid-state imaging device according to claim 5, further comprising a pixel column selection information processing circuit supplied with a signal for selecting a pixel column, for decoding the signal for selecting a pixel column; and a pixel column selection circuit supplied with a decoded output of said pixel column selection information processing circuit, for making switching between the first and second operation modes by controlling said horizontal driving circuit to output horizontal output pulses at different timings in the first and second operation modes.

7. The solid-state imaging device according to claim 5, wherein said horizontal driving circuit includes a pulse generating section for outputting a horizontal readout pulse and clear pulse.

8. The solid-state imaging device according to

claim 5, wherein said horizontal readout switching circuits include a group of transistors which are supplied with the outputs of said signal processing circuits corresponding to the vertical signal lines at one-side ends of current paths thereof and commonly connected to the horizontal signal line at the other ends of the current paths thereof and whose gates are supplied with the output signal of said horizontal driving circuit, said transistors being sequentially turned ON in the first operation mode and a plurality of transistors among said group of transistors being turned ON at substantially the same time in the second operation mode.

9. The solid-state imaging device according to claim 5, wherein each of said signal processing circuits includes a noise canceller circuit.

10. A readout method of a solid-state imaging device which includes an imaging area having unit cells arranged in a two-dimensional fashion on a semiconductor substrate, each of the unit cells including first and second photoelectric conversion/storage sections for photoelectrically converting incident light and storing charges thus generated, first and second charge readout circuits for transferring charges stored in the first and second photoelectric conversion/storage sections to a common charge detecting section, a potential detecting circuit

for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines, a reset circuit for discharging the charges transferred to the charge detecting section, and an address circuit for selectively activating the potential detecting circuit; a vertical driving circuit provided in correspondence to each pixel row of the imaging area, for driving the first and second charge readout circuits, reset circuit and address circuit of each of the unit cells at preset timings; signal processing circuits respectively attached to the vertical signal lines which are respectively provided for columns of the unit cells, for performing required signal processes; a horizontal driving circuit for scanning outputs of the signal processing circuits in a horizontal direction at preset timing to detect the same; and an output circuit for outputting output signals of the signal processing circuits detected by the scanning operation by the horizontal driving circuit; comprising the steps of:

driving the first and second charge readout circuits at substantially the same timing by use of the vertical driving circuit;

transferring the charges stored in the first and second photoelectric conversion/storage sections to the

charge detecting section and adding the charges together;

detecting the added charges by use of the potential detecting circuit;

generating a potential corresponding to an amount of the detected charges and transmitting the potential to the vertical signal line; and

outputting the potential from the output circuit via the signal processing circuit.

11. A readout method of a solid-state imaging device which has first and second operation modes and includes an imaging area having unit cells arranged in a two-dimensional fashion on a semiconductor substrate, each of the unit cells including a photoelectric conversion/storage section for photoelectrically converting incident light and storing charges thus generated, a charge readout circuit for transferring charges stored in the photoelectric conversion/storage section to a charge detecting section, a potential detecting circuit for detecting charges transferred to the charge detecting section, generating a potential corresponding to an amount of detected charges and transmitting the potential to a corresponding one of vertical signal lines, a reset circuit for discharging the charges transferred to the charge detecting section, and an address circuit for selectively activating the potential detecting circuit; a vertical driving circuit

provided in correspondence to each pixel row of the imaging area, for driving the charge readout circuit, reset circuit and address circuit of each of the unit cells at preset timings; signal processing circuits respectively attached to the vertical signal lines which are respectively provided for columns of the unit cells, for performing required signal processes; horizontal readout switching circuits for controlling transfer of outputs of the signal processing circuits corresponding to the respective vertical signal lines to a horizontal signal line; a horizontal driving circuit for controlling the horizontal readout switching circuit at preset timings; and an output circuit for outputting output signals of the signal processing circuits which are read out to the horizontal signal line by controlling the horizontal readout switching circuits by use of the horizontal driving circuit; the first operation mode comprising the steps of:

sequentially turning ON the horizontal readout switching circuits corresponding to the vertical signal lines by use of the horizontal driving circuit; and

sequentially outputting the output signals of the signal processing circuits corresponding to the vertical signal lines from the output circuit via the horizontal signal line; and

the second operation mode comprising the steps of:

turning ON the horizontal readout switching circuits corresponding to plural ones of the vertical signal lines at substantially the same time;

reading out the output signals of the signal processing circuits corresponding to the plurality of vertical signal lines to the horizontal signal line and averaging the output signals; and

outputting the averaged output signals of the signal processing circuits from the output circuit.

12. The readout method of the solid-state imaging device according to claim 11, wherein the horizontal readout switching circuits include a group of transistors whose current paths are respectively supplied at one end thereof with the outputs of the signal processing circuits corresponding to the vertical signal lines and are commonly connected at the other end thereof to the horizontal signal line and whose gates are respectively supplied with the output signals of the horizontal driving circuit, said group of transistors are controlled to be sequentially turned ON in said first step and a plurality of transistors among said group of transistors are turned ON at substantially the same time in said second step.